What is claimed is:

1. A method for automatically generating a test environment for testing a plurality of DUTs in a test system, comprising the steps of:

mapping the plurality of DUTs into pins of the tester system to create pin data;
inputting into a test program generator pattern data, generic test program rules and the pin data;
generating a multi-DUT test program and multi-DUT pattern data; and
controlling the test system through the test program.

2. The method of claim 1 also comprising the step of generating functional fail data for each DUT.

3. The method of claim 1 wherein the multi-DUT test program makes a plurality of DUTs appear as a single DUT.

4. The method of claim 1 wherein test program generation occurs independently from tester software.

5. The method of claim 1 wherein the mapping of the plurality of DUTs to the tester system pins occurs independently of restrictions imposed by the test system.

6. The method of claim 5 also comprising the step of interfacing to a generic device interface board based on channel assignments created in the mapping step.

7. An automated test system which generates test results for a plurality of DUTs using one tester, which automated test system comprises.
a pin data storage area which contains pin data which maps the plurality of DUTs into pins of the

tester system;

a pattern data storage area,
a generic program rules storage area;
a test program generator which takes as input the pin data, pattern data and generic program rules;
a multi-DUT test program which is generated by the test program;
a multi-DUT pattern data storage area generated by the the test program;
a tester containing a plurality of DUTs that has an input from the multi-DUT pattern data and is controlled by the multi-DUT test program.

8. The automated test system of claim 7 which also comprises a storage area for receiving fail data for each of the plurality of DUTs.

9. The automated test system of claim 7 where the multi-DUT pattern data is input into the tester in either serial or parallel form.

10. The automated test system of claim 7 where the multi-DUT pattern data appears to the tester as a pattern data from a single DUT.

11. The automated test system of claim 7 where pin data in the pin data storage area is mapped in a manner that would violate tester pin restrictions.

12. The automated test system of claim 7 also comprise a generic device interface board that is mapped to the tester according to the pin data.

13. A program storage device readable by automated test system, tangibly embodying a program of instructions executable by the automated test system to perform method steps for automatically

generating a test environment for testing a plurality of DUTs in a tester, said method steps comprising:

mapping the plurality of DUTs into pins of the tester system to create pin data;

inputting into a test program generator pattern data, generic test program rules and the pin data;

generating a multi-DUT test program and multi-DUT pattern data; and

controlling the tester through the test program.

14. The program storage device of claim 13 wherein the method also comprises the step of generating functional fail data for each DUT.

15. The program storage device of claim 13 wherein the multi-DUT test program makes a plurality of DUTs appear as a single DUT.

16. The program storage device of claim 13 wherein test program generation occurs independently from tester software.

17. The program storage device of claim 13 wherein the mapping of the plurality of DUTs to tester system pins occurs independently of restrictions imposed by the test system.

18. The program storage device of claim 13 wherein the multi-DUT test patterns are provided to the tester in both serial and parallel form.